Q.P. Code: 20EC0402 **R20**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B. Tech II Year I Semester Supplementary Examinations November-2022

ELECTRONIC DEVICES AND CIRCUITS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Sketch the V-I Characteristics of a PN Junction diode and illustrate its action under forward bias and reverse bias.	L3	6M
	b	What is a clamper circuit? Describe about positive and negative clampers with neat circuit diagram.	L2	6M

OR

2	a	Derive the expression for Diffusion capacitance of a PN Junction diode.	L3	6M
	b	Define and differentiate PN diode and Zener diode. Discuss different breakdown mechanisms in Zener diode.	L2	6M

UNIT-II

3	a	Demonstrate the working principle of LC filter with a circuit diagram and derive the expression for its ripple factor. List the advantages and disadvantages.	L4	6M
	b	Explain the construction, working principle and characteristics of LED with neat diagram. List the advantages and applications.	L2	6M

OR

4	a	With the help of a circuit diagram and waveforms, explain the operation of Full wave rectifier with capacitor filter and derive the expression for its ripple factor.	L3	6M
	b	Demonstrate the construction, working and characteristics of UJT with a diagram. List the applications.	L2	6M

UNIT-III

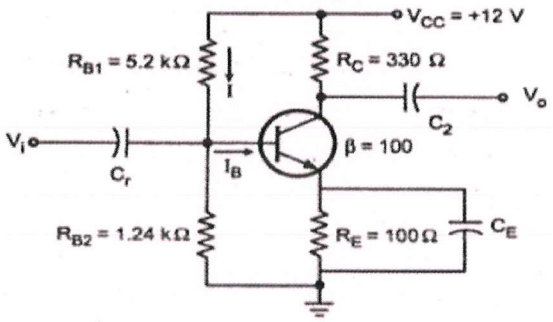
5	a	Define early effect. With a diagram, describe how a transistor acts as an amplifier.	L2	6M
	b	Discuss about the construction and working principle of N-Channel JFET along with its characteristics.	L2	6M

OR

6	a	Define three regions of BJT operation. Explain the operation of an PNP transistor.	L2	6M
	b	Differentiate the MOSFET with FET and explain the N-channel enhancement type MOSFET with characteristics.	L2	6M

UNIT-IV

7	a	Draw the DC load line and obtain quiescent point for the transistor shown below.	L4	6M



	b	Define thermal stability. Estimate the condition for achieving thermal stability.	L3	6M

OR

8	a	Draw the circuit diagram of Self Bias of a Transistor and determine its Q-point.	L3	6M
	b	Explain diode compensation technique for the parameters of V_{BE} and I_{CO}.	L2	6M

UNIT-V

9	a	Examine the expressions for current gain, voltage gain, input impedance and output impedance of CB amplifier using simplified hybrid model.	L4	6M
	b	Draw the circuit diagram of JFET Common Source amplifier with voltage divider bias for bypassed Rs and determine the expression for input impedance, output impedance and voltage gain.	L3	6M

OR

10	a	A voltage source of internal resistance, Rs = 900Ω drives a CC amplifier using load resistance RL=2000Ω. The CE h parameters are hfe=60, hie=1200Ω, hoe = 25μA/V and hre = 2×10^{-4}. Calculate AI, Ri, Av and R0 using approximate analysis.	L4	6M
	b	Summarize the expressions for input impedance, output impedance and voltage gain of JFET Common Drain amplifier with neat diagram.	L3	6M

*** END ***